

Receipt date: 10/01/2009

Doc code: IDS

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PTO/SB/08a (06-09)

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> ( Not for submission under 37 CFR 1.99)	Application Number	09989762
	Filing Date	2001-11-19
	First Named Inventor	Kenneth Y. Ogami
	Art Unit	2123
	Examiner Name	Luke R. Osborne
	Attorney Docket Number	CDO1175M

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code <sup>1</sup>	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	6828824	B1	2004-12-07	Betz et al.	Entire Document
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	3	4942540	B1	1990-07-17	Black et al.	Entire Document
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10	6366300	B1	2002-04-02	Ohara et al.	Entire Document
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21	5136188	B1	1992-08-04	Ha et al.	Entire Document
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24	5422823	B1	1995-06-06	Agrawal et al.	Entire Document
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**U.S.PATENT APPLICATION PUBLICATIONS**

Examiner Initial*	Cite No	Publication Number	Kind Code <sup>1</sup>	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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	2	20070139074	A1	2007-06-21	Reblewski, Frederic	Entire Document

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**FOREIGN PATENT DOCUMENTS**

Examiner Initial*	Cite No	Foreign Document Number <sup>3</sup>	Country Code <sup>2</sup>	Kind Code <sup>4</sup>	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T <sup>5</sup>
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**NON-PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>5</sup>
	1	Kory Hopkins, "Definition;" 01/16/1997; < <a href="http://www.cs.sfu.ca/cs/people/GradStudent.html">http://www.cs.sfu.ca/cs/people/GradStudent.html</a> >; 1 page	<input type="checkbox"/>
	2	Ebeling et al., "Validating VLSI Circuit Layout by Wirelist Comparison;" Sept. 1983; in proceedings of the IEEE International Conference on Computer Aided Design (ICCAD-83); 2 pages	<input type="checkbox"/>
	3	USPTO Notice of Allowance for Application Number 11/986,338 (CD1197C) dated 05/07/2009; 1 page	<input type="checkbox"/>
	4	Ohlrich et al., "Sub-Gemini: Identifying Subcircuits using a Fast Subgraph Isomorphism Algorithm;" June 1993; in proceedings of the 30th IEEE/ACM Design Automation Conference; 7 pages	<input type="checkbox"/>
	5	Ebling, "Gemini II: A Second Generation Layout Validation Program;" 1988; in proceedings of the IEEE International Conference on Computer Aided Design (ICCAD-88); 4 pages	<input type="checkbox"/>
	6	Application Number 11/965,291 (CD2007130): "Universal Digital Block Interconnection and Channel Routing," Snyder et al., filed on 12/27/2007; 31 pages	<input type="checkbox"/>
	7	Application Number 12/356,468 (CD01174D): "System and Method for Dynamically Generating a Configuration Datasheet," Anderson et al.; filed on 01/20/2009; 27 pages	<input type="checkbox"/>
	8	International Search Report from the International Search Authority for International Application Number PCT/US08/60680 (CD2007130PCT) dated 08/15/2008; 4 pages	<input type="checkbox"/>

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9	USPTO Notice of Allowance for Application Number 09/475,879 (CD99047) dated 10/22/2004; 7 pages	<input type="checkbox"/>
10	USPTO Advisory Action for Application Number 09/475,879 (CD99047) dated 03/04/2002; 3 pages	<input type="checkbox"/>
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14	Application Number 09/475,879 (CD99047): "Programmable Logic Device," Lacey et al.; filed on 12/30/1999; 50 pages	<input type="checkbox"/>
15	Application Number 09/475,808 (CD99069): "Configurable Memory for Programmable Logic Circuits," Lacey et al.; 24 pages 12/30/99	<input type="checkbox"/>
16	USPTO Non-Final Rejection for Application Number 09/475,808 (CD99069) dated 06/06/2001; 8 pages	<input type="checkbox"/>
17	USPTO Notice of Allowance for Application Number 09/475,808 (CD99069) dated 11/06/2001; 8 pages	<input type="checkbox"/>
18	Application Number 10/137,497 (CD01197M): "Reconfigurable Testing System and Method," Pleis et al.; filed on 05/01/2002; 40 pages	<input type="checkbox"/>
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20	USPTO Final Rejection for Application Number 10/137,497 (CD01197M) dated 05/05/2005; 13 pages	<input type="checkbox"/>
21	USPTO Non-Final Rejection for Application Number 10/137,497 (CD01197M) dated 09/22/2005; 21 pages	<input type="checkbox"/>
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26	Application Number 10/653,050 (CD01242C): "Method and System for Programming a Memory Device," Snyder et al.; filed on 08/29/2003; 69 pages	<input type="checkbox"/>
27	USPTO Non-Final Rejection for Application Number 10/653,050 (CD01242C) dated 04/06/2004; 7 pages	<input type="checkbox"/>
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29	Application Number 10/172,670 (CD01242M): "Method and System for Programming a Memory Device," Snyder et al.; filed on 06/13/2002; 66 pages	<input type="checkbox"/>
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**EXAMINER SIGNATURE**

Examiner Signature	/Luke Osborne/	Date Considered	10/14/2009
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